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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/755,572	01/08/2001	Ting Cheong Ang	CS99-224	3795

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EXAMINER
FOONG, SUK SAN

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 03/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No	Applicant(s)	
	09/755,572	ANG ET AL.	
	Examiner	Art Unit	
	Suk-San Foong	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2002*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 8-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 8-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 November 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a)☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
4)☐ Interview Summary (PTO-413) Paper No(s) _____
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1, 2 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Babcock et al. ('155) in combination with Kunikiyo ('087) and Matsumoto et al. ('397).

Babcock et al. teaches a method of forming a SOI (silicon-on-insulator) device for integrated circuits which includes providing silicon layer 265 over oxide layer 280 on a silicon semiconductor substrate 290 (Paragraph [0021]), then forming first trench 275 in silicon layer 265 wherein first trench 275 extends partially through silicon layer 265, does not extend through to underlying oxide layer 280 and no implant is made underlying first trench 275 (Paragraph [0022], and Figs. 2B and 4B), subsequently filling first trench 275 with an insulating layer such as oxide (Paragraph [0022]), then etching second trenches 270 into silicon layer 265 wherein second trenches 270 extend fully through silicon layer 265 to oxide layer 280 thereby isolating active areas of substrate 290 and wherein first trench 275 lies in active areas (Paragraphs [0022, 0027, 0028], and Figs. 2B, 4A and 4B), then filling second trenches 270 with insulating layer such as oxide (Paragraph [0022]), subsequently forming gate electrodes 200 or 510 (Paragraph [0023], and Figs. 2B and 4B), then forming source and drain regions 220, 210 or 490, 500 (Paragraph [0023], and Figs. 2B and 4B), and then forming second contact 225 or 510 between first trench 275 and one of second trenches 270 (Paragraph [0028], and Figs. 2B and 4B)

Babcock et al. does not teach depositing an interelevel dielectic layer overlying gate electrodes.

Babcock et al. does not teach forming first contacts through the interlevel dielectric layer to underlying source and drain regions.

Babcock et al. does not teaching forming second contact through the interlevel dielectric layer.

Kunikiyo teaches a method of forming a semiconductor device with SOI structure which includes providing silicon substrate 113 (Col. 1, line 31 and lines 41-43, and Figs. 16 and 20), forming oxide layer 114 over substrate 113 (Col. 1, line 29), then forming silicon layer 115 over oxide layer 114 (Col. 1, line 31), etching silicon layer 115 to form first trench 116 (Fig. 16) and filling with insulating layer (Col. 2, lines 6-16), etching silicon layer 115 to form second trenches 150 (Fig. 16) filling with insulating layer (Col. 1, lines 44-49), then forming gate electrode 119 and source and drain regions 124 on silicon layer 115 (Fig. 16 and Fig. 4), then forming interlevel insulating layer 127 (Fig. 16, and Col. 3, lines 27), forming first contact plugs 131 and 129 through interlevel insulating layer 127 to source and drain regions 124 (Fig. 4, and Col. 3, lines 2-4), and forming second body contact 135 between first trench 116 and one of second trenches 150 (Fig. 16).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Babcock et al. with Kunikiyo because it would enable formation of second contact 225 or 510 of Babcock et al. to be performed through interlevel insulating layer 127 of Kunikiyo.

It would have been within the scope to one ordinary skill in the art to combine the teachings of Babcock et al. with Kunikiyo to employ formation of first contact plugs 131 and

129 through the interlevel insulating layer of Kunikiyo to source and drain regions 220, 210 or 490, 500 of Babcock et al.

The combination process does not teach that the second contact is contacting both first and second trenches.

Matsumoto et al. discloses a method of forming a semiconductor devices having a SOI structure wherein contact 1010 is formed so as to extend over the surface of isolation regions 104 (Paragraph [0008], and Fig. 22).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Matsumoto et al. with the combination process because it would enable formation of contact 225 or 501 of the combination process to be performed and obtain further advantage of improving element density (Matsumoto et al., Paragraph [0008]).

The choice of trench depth would be a matter of routine optimization to achieve the desired device dimensions and the desired device characteristics of the device to be formed. (See MPEP 2144.05).

3. Claims 3 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Babcock et al. ('155) in combination with Kunikiyo ('087) and Matsumoto et al. ('397) as applied to claims 1, 2 and 8 above, and further in view of Chen et al. ('941).

The combination process does not teach that trenches are filled with a liner oxide.

Chen et al. disclose a method of forming trench isolation on SOI substrate which includes forming silicon substrate 52 of SOI structure (Col. 3, lines 10-12), then sequentially depositing pad oxide layer 62 and silicon nitride layer 64 to form hard mask for subsequent etching process

(Col. 3, lines 12-14), then etching silicon substrate 52 to form trench 54 (Col. 3, lines 18-21 and Fig. 3), then forming silicon dioxide liner layer 72 in trench 54 (Col. 3, lines 34-38, and Fig. 4), and filling trench 54 with insulating material 74 (Col. 3, lines 62-65) such as oxide (Col. 2, lines 44-46).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Chen et al. with the combination process because it would enable formation of insulated trenches 270 and 275 by depositing liner oxide in trench openings and to obtain further advantages of effective corner-rounding and improved gap filling ability (Chen et al., Col. 4, lines 12-16).

4. Claims 4, 5, 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Babcock et al. ('155) in combination with Kunikiyo ('087) and Matsumoto et al. ('397) as applied to claims 1, 2 and 8 above, and further in view of Wolf.

The combination process does not teach the recited interlevel insulating layer materials.

Wolf teaches a method forming interlevel dielectric layers in semiconductor device which includes providing dielectric layer consisting of TEOS material (page 194) over metal or polysilicon layers.

It would have been within the scope to one ordinary skill in the art to combine the teachings of Wolf with the combination process because it would enable formation of interlevel insulating layer 127 of the combination process and to obtain further advantage of excellent step coverage (page 194).

The choice of thickness of interlevel dielectric layer would be a matter of routine optimization to achieve the desired device dimensions and the desired device characteristics of the device to be formed. (See MPEP 2144.05).

With respect to claims 5 and 11, the combination process does not teach that conducting layer is comprised of tungsten or aluminum-copper alloys.

Wolf discloses an array of conductive materials for forming contacts between interlevel insulating layers which includes filling contact holes and vias with tungsten (page 192).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Wolf with combination process because it would enable formation of contact plugs 131 and 129 of the combination process to be performed.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suk-San Foong whose telephone number is 703-305-0383. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 (7724, 3431, 3432).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

sf
February 24, 2003

George Fourson
Primary Examiner
Art Unit 2823